REMARKS

Claims 1 through 13 remain pending. In response to the final Office Action dated November 1, 2005, the specification and claims 1 and 11 are amended, and a Request for Continued Examination and two replacement drawing sheets are submitted. Care has been taken to avoid adding new matter. A petition for two month extension of the period for response, with appropriate fee charge authorization, is filed herewith. Favorable reconsideration of the application is respectfully solicited.

Claims 1 and 11 were rejected under the first paragraph of 35 U.S.C. § 112. The logic functionality recited in the claims was held to lack enabling support in the disclosure. In response, the disclosure has been again reviewed. Errors have been found in the depicted comparator input ports in Figs. 1 and 3. From the claim requirement that the detection signals are output when the detected gate and collector levels exceed the reference signals, it is clear that the comparator input ports to which the reference signals are applied should be the inverting input ports and the other input ports should be the noninverting input ports. Figs. 1 and 3 thus contain errors that have been corrected in the replacements sheets submitted herewith. The specification has been amended at pages 7, 8 and 12 to be consistent with these drawing corrections.

Additional basis in the original disclosure for above discussed corrections can be found, for example, at page 8, lines 11-15. As described therein, the logic AND circuit outputs a high logic level when both of its inputs are a high logic level. The COMP 1 and COMP 2 outputs are input to the AND circuit and must be at high logic levels for the AND circuit to produce the high logic level output. It is submitted, therefore, that the present amendment meets the requirements of 35 U.S.C. § 112. Withdrawal of the rejection is respectfully solicited.

Claims 1 through 4 were again rejected under 35 U.S.C. § 102(b) as being anticipated by Kimura, of record. In response, independent claim 1 (as well as independent claim 11) is amended to recite that the second reference voltage, to which the detected gate signal is compared, is produced on the basis of a potential at the emitter of said power semiconductor device.

The second comparator compares the gate voltage of the trench type power semiconductor device with the second reference voltage which is produced on the basis of a potential at the emitter of said power semiconductor device and set to be lower than a line power voltage of a drive circuit for outputting a drive signal that drives said power semiconductor device and higher than a terraced voltage of the power semiconductor device. The second comparator outputs a second detection signal when the detected gate signal exceeds a second reference voltage. As shown in Figs. 1 and 3, the second reference voltage V2 is connected to the same potential (GND) of the emitter terminal of IGBT 1. This means that the second reference voltage is produced on the basis of a potential at the emitter of said power semiconductor device. The second reference voltage is set to be lower than a line power voltage of a drive circuit for outputting a drive signal that drives said power semiconductor device and higher than a terraced voltage of the power semiconductor device. See Fig. 2. The second reference voltage V2 for detecting a gate voltage is set to be lower than the gate drive circuit line voltage, which is, for example, 15V, and to be a terraced voltage of the IGBT 1 or over (terraced voltage + α). During normal switching, when a collector voltage collection signal is being output, no gate voltage detection signal is set to be output from the second comparator COMP 2. See page 10, lines 1-8 of the original specification. Such circuit configuration is very suitable for

the protection of the trench-type power semiconductor device which has a low gate threshold voltage. See page 2, lines 23-28 of the original specification.

Kimura teaches comparing the gate voltage with a reference voltage which is the line power voltage (the power supply voltage) of the drive circuit as mentioned on page 2, lines 18-22 of our specification. Fig. 8 of Kimura also shows that the second over-current detection signal is generated based on the difference between the gate voltage (VG) of IGBT 10 and the power supply voltage (1, 2). There is a problem in such circuit configuration. If the power supply voltage is set as a reference voltage to determine a short circuit in the gate voltage of a device which has a low threshold voltage, or has a large current gain, such as a trench IGBT, when a short circuit is detected, the gate voltage is in a state wherein the power supply voltage of a gate drive circuit, for example 15V, has been applied thereto. In the state wherein the power supply voltage of the gate drive circuit is applied, an excessive short circuit current flows that is several tens times the device rated current. Kimura does not teach that the second reference voltage is produced on the basis of a potential at the emitter of said power semiconductor device. Kimura also does not teach that the second reference voltage is set to be lower than a line power voltage of a drive circuit for outputting a drive signal that drives said power semiconductor device and higher than a terraced voltage of the power semiconductor device. Kimura is not concern with the terraced voltage.

For the above stated reasons, the rejection as it may be applied to the claims as now amended, is respectfully traversed. Withdrawal of the rejection is respectfully solicited.

Claims 1, 3 and 4 were further rejected, and claims 9 and 10 were rejected, under 35 U.S.C. § 103(a) as being unpatentable over Kimura in view of U.S. published application 2004/0075103 (Topp). The Office Action recognizes that Kimura does not disclose a trench type

power semiconductor device. Topp has been relied upon for disclosing a trench IGBT. It was concluded that it would have been obvious to modify the Komura device "by adding the trench type IGBT according to Topp." This position, and the rejection, are respectfully traversed.

As stated in the section 0018 of Topp et al., IGBY 100 is a vertical IGBT (V-IGBT) which is *not* a trench type IGBT. A trench-type semiconductor device is formed with a trench in the semiconductor substrate and the device element such as a gate is formed in the trench. Reference is made to U.S. patent 6,323,518 and U.S. patent 6,180,966 as examples of trench-type semiconductor devices. Kimura et al. and Topp do not concern the specific problem of the over-current protection for the trench-type power semiconductor device. It is submitted, therefore, that the modification propounded as obvious in the Office Action would not have resulted in the claimed invention. Withdrawal of the rejection is respectfully solicited.

Claim 2 was rejected under 35 U.S.C. § 103(a) as being unpatentable over Kimura in view of Topp and further in view of U.S. patent 5,650,906 (Marquardt). Claim 2 is dependent from claim 1 and further recites a voltage divider. Marquardt has been relied upon for concluding that the additional requirement of claim 2 would have been obvious in the proposed Kimura/Topp combination.

Claims 5 through 8 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Kimura in view of Topp and further in view of Horowitz, of record. Claims 5 through 8 also are dependent from claim 1. Horowitz has been relied upon solely for the added requirements of the dependent claims.

It is submitted, however, that Marquardt and Horowitz do not disclose, nor have they been relied upon for disclosing, the trench type power semiconductor device features of claim 1,

described above. It is submitted, therefore, that claims 2 and 5 through 8 are patentably distinguishable from the applied references, taken singly or in combination.

Claims 11 through 13 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Kimura in view of Topp and further in view of Wacknov, of record. Claims 12 and 13 are dependent from claim 11. Kimura, Topp and Wacknov, considered singly or in combination, do not teach that the second reference voltage for detecting the over-current of the gate is set to be lower than a line power voltage of a drive circuit and higher than a terraced voltage of the power semiconductor device. Wacknov is not concerned with the terraced voltage. It is submitted, therefore, that claims 11 through 13 are patentably distinguishable.

Allowance of the application is respectfully solicited. To the extent necessary, a petition for an extension of time under 37 C.F.R. 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account 500417 and please credit any excess fees to such deposit account.

Respectfully submitted,

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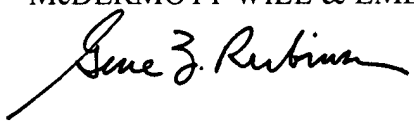

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